

# 8-bit compatible shift / store register

## BU4094BC / BU4094BCF / BU4094BCFV

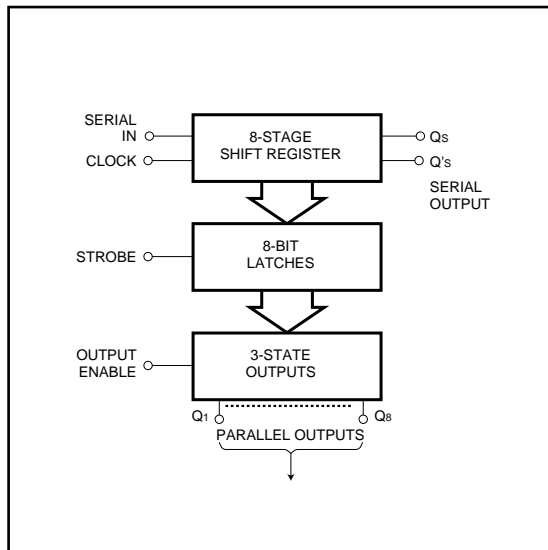
The BU4094BC, BU4094BCF, and BU4094BCFV are shift / store registers, each consisting of an 8-bit register and an 8-bit latch.

As the data in the shift register can be latched by an asynchronous strobe input, it is possible to hold the output in the data transfer mode.

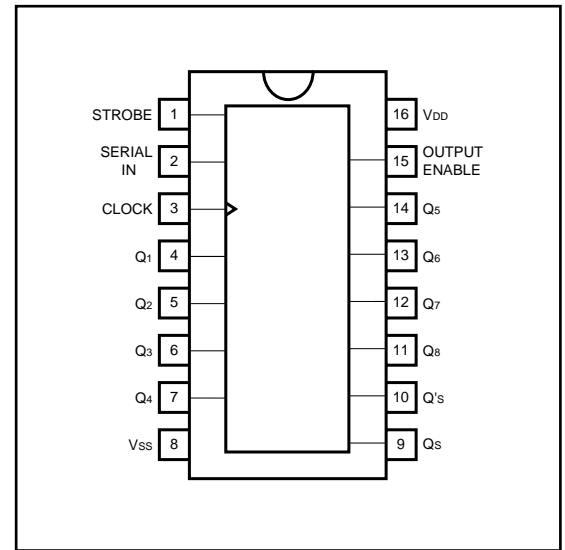
The tri-state parallel output can be connected directly with an 8-bit bus line.

These registers are suitable for in-line / parallel data conversion, data receivers and other similar applications.

●Logic circuit diagram



●Block diagram



●Truth table

CLOCK	OUTPUT ENABLE	STROBE	SERIAL IN	Parallel output		Serial output	
				Q <sub>1</sub>	Q <sub>n</sub>	Q <sub>s</sub>	Q' <sub>s</sub>
$\text{—}\overline{\text{f}}$	H	H	L	L	Q <sub>n-1</sub>	Q <sub>7</sub>	NC
$\text{—}\overline{\text{f}}$	H	H	H	H	Q <sub>n-1</sub>	Q <sub>7</sub>	NC
$\text{—}\overline{\text{f}}$	H	L	X	NC	NC	Q <sub>7</sub>	NC
$\text{—}\overline{\text{f}}$	L	X	X	Z	Z	Q <sub>7</sub>	NC
$\text{—}\overline{\text{f}}$	H	X	X	NC	NC	NC	Q <sub>s</sub>
$\text{—}\overline{\text{f}}$	L	X	X	Z	Z	NC	Q <sub>s</sub>

NC: No Change Z: High Impedance X: Irrelevant

## ●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	- 0.5 ~ + 20	V
Power dissipation	P <sub>d</sub>	1000 (DIP), 500 (SOP) 400 (SSOP)	mW
Operating temperature	T <sub>opr</sub>	- 40 ~ + 85	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ + 150	°C
Input voltage	V <sub>IN</sub>	- 0.5 ~ V <sub>DD</sub> + 0.5	V

## ●Electrical characteristics

DC characteristics (unless otherwise noted, V<sub>SS</sub> = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V <sub>DD</sub> (V)	Conditions
Input high level voltage	V <sub>IH</sub>	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input low level voltage	V <sub>IL</sub>	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input high level current	I <sub>IH</sub>	—	—	0.3	μA	15	V <sub>IH</sub> = 15V
Input low level current	I <sub>IL</sub>	—	—	- 0.3	μA	15	V <sub>IL</sub> = 0V
Output high level voltage	V <sub>OH</sub>	4.95	—	—	V	5	I <sub>o</sub> = 0mA
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	V <sub>OL</sub>	—	—	0.05	V	5	I <sub>o</sub> = 0mA
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	I <sub>OH</sub>	- 0.44	—	—	mA	5	V <sub>OH</sub> = 4.6V
		- 1.1	—	—		10	V <sub>OH</sub> = 9.5V
		- 3.0	—	—		15	V <sub>OH</sub> = 13.5V
Output low level current	I <sub>OL</sub>	0.44	—	—	mA	5	V <sub>OL</sub> = 0.4V
		1.1	—	—		10	V <sub>OL</sub> = 0.5V
		3.0	—	—		15	V <sub>OL</sub> = 1.5V
Output high level disable current	I <sub>DH</sub>	—	—	1.0	μA	15	V <sub>OUT</sub> = 15V
Output low level disable current	I <sub>DL</sub>	—	—	- 1.0	μA	15	V <sub>OUT</sub> = 0V
Static current dissipation	I <sub>DD</sub>	—	—	20	μA	5	V <sub>I</sub> = V <sub>DD</sub> , or GND
		—	—	40		10	
		—	—	80		15	

Switching characteristics (unless otherwise noted,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $C_L = 50pF$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	V <sub>DD</sub> (V)	Conditions	Measurement circuit
Output rise time	t <sub>RLH</sub>	—	100	—	ns	5	—	Fig.1
		—	50	—	ns	10		
		—	40	—	ns	15		
Output fall time	t <sub>RHL</sub>	—	100	—	ns	5	—	Fig.1
		—	50	—	ns	10		
		—	40	—	ns	15		
Propagation delay time, CLOCK to Qs	t <sub>PLH</sub> t <sub>PHL</sub>	—	350	600	ns	5	—	Fig.1
		—	125	250	ns	10		
		—	95	190	ns	15		
Propagation delay time, CLOCK to Qs	t <sub>PLH</sub> t <sub>PHL</sub>	—	230	460	ns	5	—	Fig.1
		—	110	220	ns	10		
		—	75	150	ns	15		
Propagation delay time, CLOCK to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	—	420	840	ns	5	—	Fig.1
		—	195	390	ns	10		
		—	135	270	ns	15		
Propagation delay time, STROBE to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	—	290	580	ns	5	—	Fig.1
		—	145	290	ns	10		
		—	100	200	ns	15		
3-state propagation delay time, Output Enable to Qn	t <sub>PHZ</sub> t <sub>PZH</sub>	—	140	280	ns	5	R <sub>L</sub> = 1k $\Omega$	Fig.2
		—	75	150	ns	10		
		—	55	110	ns	15		
3-state propagation delay time, Output Enable to Qn	t <sub>PLZ</sub> t <sub>PZL</sub>	—	140	280	ns	5	R <sub>L</sub> = 1k $\Omega$	Fig.2
		—	75	150	ns	10		
		—	55	110	ns	15		
Minimum setup time, DATA to CLOCK	t <sub>su</sub>	—	20	125	ns	5	—	Fig.1
		—	8	55	ns	10		
		—	6	35	ns	15		
Minimum hold time, CLOCK to DATA	t <sub>h</sub>	—	10	40	ns	5	—	Fig.1
		—	10	20	ns	10		
		—	5	15	ns	15		
Minimum clock pulse width	t <sub>w</sub>	—	100	200	ns	5	—	Fig.1
		—	50	100	ns	10		
		—	40	80	ns	15		
Maximum clock rise time and fall time	t <sub>r(CL)</sub> t <sub>f(CL)</sub>	NO Limit			$\mu$ s	5	—	Fig.1
					$\mu$ s	10		
					$\mu$ s	15		
Maximum clock frequency	f <sub>CL</sub>	1.25	5	—	MHz	5	—	Fig.1
		2.5	10	—	MHz	10		
		3.0	12.5	—	MHz	15		
Minimum strobe pulse width	t <sub>WH</sub>	—	100	200	ns	5	—	Fig.1
		—	40	80	ns	10		
		—	35	70	ns	15		
Input capacitance	C <sub>IN</sub>	—	5	—	pF	—	—	—

● Measurement circuits

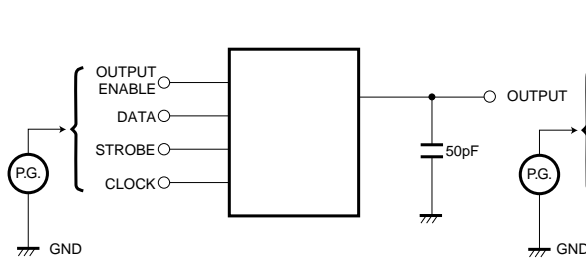


Fig. 1 Switching waveform

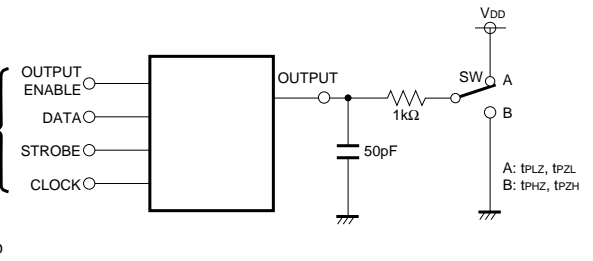


Fig. 2 3-state delay time

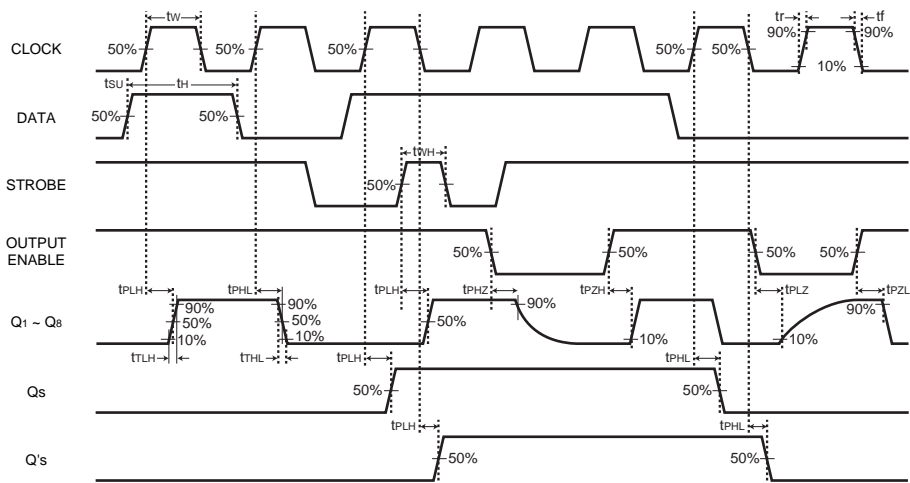


Fig. 3 Switching time test waveform

● Electrical characteristic curve

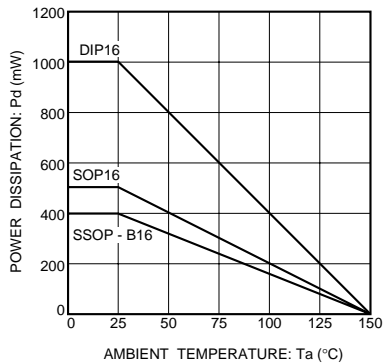


Fig. 4 Power dissipation vs. ambient temperature

●External dimensions (Units: mm)

