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SERVICE MANUAL

GOLDEN EAGLE MARK IV

TABLE OF CONTENTS

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LACONIA, N.H. 03246

(603) 524-5454

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BROWNING LABORATORIES, INC.

Box 310

LACONIA, NH 03246

MARK IV SERVICE MANUAL

SECTION 1

GENERAL INFORMATION

1.1 SCOPE OF THIS MANUAL

This service manual contains complete servicing alignment and troubleshooting instructions for the Golden Eagle MARK IV Base Station.

1.2 FACTORY SERVICE & RETURNS

Browning maintains a National Customer Service Department for your assistance. This department is available for consultation, assistance on technical problems, parts information or orders, and the availability of local factory authorized repair facilities. It will also assist you and coordinate returns to the factory.

For any of the above information or requirements call National Service Manager, at 603-524-5454, Ext. 36 or write:

Service Department Browning
Laboratories, Inc.
P. O. Box 310
Laconia, NH 03246

1.3 PARTS ORDERS

Browning Authorized Service Centers stock the more commonly needed replacement parts. Should a part not be available locally, it may be ordered from the National Customer Service Department. When ordering, please supply the following information:

A. Model Number of the Unit.

B. Serial Number of the Unit

C. Description of the Part.

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GOLDEN EAGLE MARK IV

SPECIFICATIONS

2.1 GENERAL

Frequency Range: 26.965 - 27.405 MHz.

Number of Channels: 40

Dimensions: Receiver: 6.75"H x 15.50"W x 9.88"D

Transmitter: 6.75"H x 15.50"W x 9.88"D

Total Shipping Weight: 51 lbs.

Microphone: Browning Model 776 High Impedance Desk Style with Push-to-Talk Bar.

Compliance: FCC Type Accepted

2.2 RECEIVER

Sensitivity: 0.3 uV for 10 dB S+N/N AM

0.1 uV for 10 db S+N/N SSB

Selectivity: 65 dB minimum at +/- 10 KHz AM

65 dB minimum at +/- 5 KHz SSB

Audio Output: 4W RMS into 3.2 ohm load.

Squelch Sensitivity: 0.8 uV Threshold

Noise Limiters (2) : SSB-Pulse Diode Type.

AM -Series Gate Type.

AGC: Less than 9 dB Audio Change Over Full Range with Front Panel defeat switch.

Frequency Range: Continuous 40 Channel tuning with separate bandspread control + HF Band to 27.595 MHz.

Circuitry: 10 Tubes, 12 Diodes, 3 Transistor & 6 LED's

Intermediate Frequencies: 1st IF = (4.435 - 4.145 MHz)

2nd IF = 455 kHz.

Modes: AM and Upper and Lower Sideband.

SECTION 2

SPECIFICATIONS

2.3 TRANSMITTER:

Emission:	AM and Upper and Lower Sideband
Frequency Control:	>/=0.005% True PLL Circuit from -30°C to 50°C
RF Power Output:	SSB 12W PEP at 117V AC
	AM 3.5W Minimum at 117V AC
RF Spurious and Harmonic Attenuation:	Better than -60 Db
Output Impedance:	50 ohms (nominal)
Modulation Capability (AM):	Limited to 100%
Carrier Suppression:	Better than -70 Db Frequency
Range:	26.965 to 27.405 Mhz
Circuitry:	8 Tubes, 25 IC's, 39 Diodes, 11 Transistors, 1 FET and 4 LED's

INSTALLATION

3.1 GENERAL

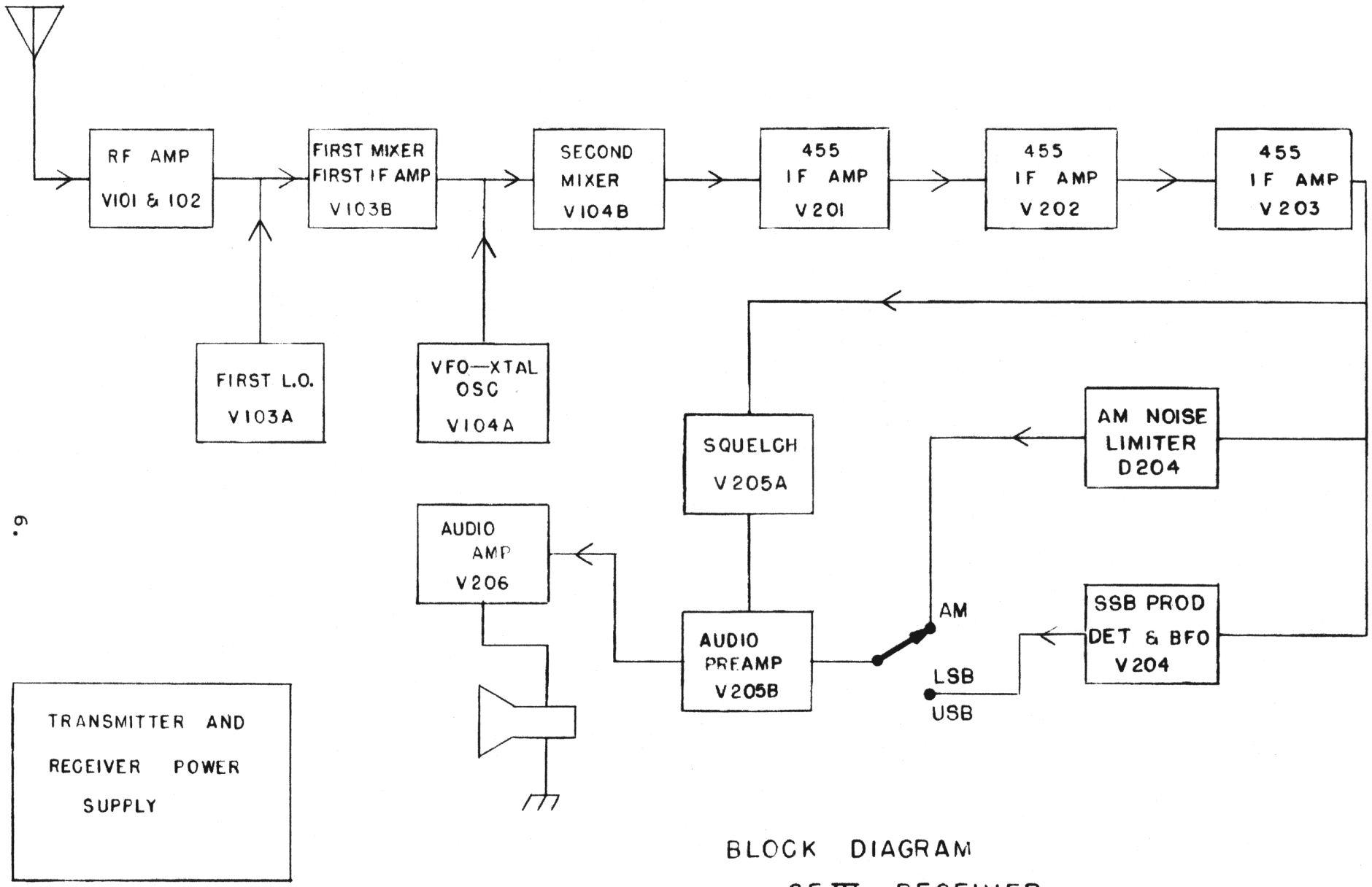
Of all the factors involved in the installation,the selection and placement of a good antenna is essential for satisfactory performance of the Golden Eagle MK-IV. Select the antenna location carefully. Install the antenna in an unobstructed area and as high as legally allowed. The feedline should also be carefully selected and low loss foam RG-8U coax is recommended, especially if a long feedline is required. A low VSWR is also important to get the maximum transmitter power to the antenna.

The placement of the Golden Eagle MK-IV Base Station should be placed for best operating ease and convenience. The transmitter and receiver should be placed side-by-side and not stacked. Stacking the units will cause excessive heat and the receiver frequency stability will be adversely affected.

Proper grounding and lightning protection is a must to reduce atmospheric noises and possible damage to the equipment. The use of inline coaxial lightning protectors will eliminate damage from electrical static charges but will not necessarily offer protection from a direct hits. Removing the antenna coax from the unit and grounding both center and outer portions and also unplugging the line cord is the best protection, this of course should only be done during an electrical storm.

Connect the Control Cable from the Transmitter to the polarized connector on the Receiver. Connect the antenna cable with PL259 plug from the transmitter to the "ANT" connector on the Receiver. Connect the outside antenna to the "ANT" connector on the Transmitter. Connect the microphone to the transmitter.

Be sure that the receiver POWER switch is in the "OFF" position and then plug the AC Line cord into the 117V AC outlet. The Golden Eagle MK-IV is now ready to be placed into service.



BLOCK DIAGRAM

GE IV RECEIVER

FIGURE 4.1

SECTION 4

CIRCUIT DESCRIPTION

4.1 GENERAL

While studying the circuit description it may be desirable to refer to the block diagram (Figures 4.1 & 4.2) as well as the complete schematics, found in the back of the manual, for a better understanding of the circuitry involved.

4.2 RECEIVER

4.2.1 GENERAL

The Golden Eagle MK-IV Receiver is continuously variable from 26.965 - 27.405 MHz (Channels 1 - 40) and 27.415 -27.595 MHz (HF band). A highly accurate dial and stable variable oscillator allow precise frequency selection. The receiver, a dual conversion super heterodyne, with intermediate frequencies of (4.435 - 4.145 MHz) and 455 KHz. All interstage transformers are double-tuned. A switchable AGC circuit is incorporated and two separate noise limiters are used, one for SSB (Pulse diode type) and one for AM (series gate type).

4.2.2 RF AMPLIFIER

During the receive condition the incoming RF signal from the antenna passes through a set of contacts on the Transmit-Receive relay (K-601) in the Transmitter, to the Receiver, to the tap on L101. Transformer L101 furnishes impedance matching and RF tuning. V101 and V102 are low noise cascaded Nuvistors and provide RF amplification. From the plate of V102, the signal is coupled into T101, a 27 MHz transformer. The output of T101 supplies the 27 MHz energy to the grid of the 1st mixer, V103B.

RF Gain Control is achieved by changing the cathode bias On V101 via R4

AGC voltage is fed to the grid of V101 and is switched in Or out via SW-2 (Part of RF Gain Control).

SECTION 4

CIRCUIT DESCRIPTION (cont'd)

4.2.3 FIRST LOCAL OSCILLATOR

V103A utilized third overtone crystals and with the plate tank circuit (L103 and C111), make up the first L.O. In the "CB-1" and "XTAL" positions of SW1-C, V103A generates the frequency of-22.82 MHz via crystal CR501. In the "CB-2" position of SW1-C. V103A generates the frequency of 23.14 MHz via crystal CR502. Depending on the position of SW1-C, 22.82 or 23.14 MHz is supplied to the grid of the first mixer, V103B.

4.2.4 FIRST MIXER

V103B performs as a mixer and combines its two inputs (received frequency and either 22.82 or 23.14 MHz). The desired resultant is: for "CB-1" or "XTAL," Received frequency - 22.82 MHz = 4.435 - 4.145 MHz; or for "CB-2," Received frequency - 23.14 MHz = 4.435 - 4.145 MHz. The 4 MHz frequency is the first IF and passes through T102 to the grid of the second mixer, V104B.

4.2.5 MANUAL OSCILLATOR

V104A, the manual oscillator or variable frequency oscillator (VFO), is a series resonant Colpits oscillator operating in the range of 4.890 to 4.600 MHz. Bandspread is achieved by varying a small D.C. voltage to D101. D101 acts as a varactor diode and changes it capacitance depending on the voltage impressed across it. V104A, also performs as a crystal oscillator when SW1 - A and B are placed into the "XTAL" position. The crystal is used only for fixed frequency monitoring in the AM mode. The output from the grid of V104A is coupled to the grid of the second mixer, V104B.

4.2.5 2nd MIXER

V104B performs as a mixer and combines its two inputs; 1st IF (4.435 - 4.145 MHz) and the VFO freq. (4.890 - 4.600 MHz) The desired resultant frequency is 455 KHz. The 455 KHz is the 2nd IF. The 455 KHz passes through two double-tuned transformers, T201 and T202, to the grid of the first IF amplifier V201.

4.2.7 455 KHz IF AMPLIFIERS & AGC

The IF amplifiers, V201, V202, and V203 raise the output of the second mixer to a level suitable for detection by either the AM detector, D202 or the SSB product detector, V204. AGC voltage is developed by D203. The AGC voltage is fed to the IF amplifiers (via R209, 205 and 201.) and the RF amplifier, via R101. IF gain control is supplied to V202 through R206 and from the RF gain control, R4.

The "S" meter develops its voltage from the cathode of V203 and R2 sets the "S" meter zero.

V204 also performs as a Beat Frequency Oscillator (BFO) for carrier injection into the product detector for modulation detection in the SSB modes. SW2-E selects the proper variable capacitor that is preset for the correct BFO frequency, depending on which sideband has been selected.

4.2.8 AUTOMATIC NOISE LIMITERS

The AM Automatic Noise Limiter (ANL) circuit consists of; R216, R217, 218 and 219: C219 and 220 and D204. The SSB ANL consists of R241 and R220, C222 and diode package, D205.

4.2.9 SQUELCH

R.7, the squelch control, adjusts the voltage to the cathode of the squelch tube, V205A. When the voltage from the last IF transformer is below a certain level(determined by the adjustment of R7), V205A will go into conduction and through the network of R230, 231, 232 and 233 will change the bias to the grid of V205B and will cut V205B off. When the level of detected audio now exceeds a certain value, V205B will go back into conduction and amplify the detected audio.

4.2.10 AUDIO AND TONE CONTROL

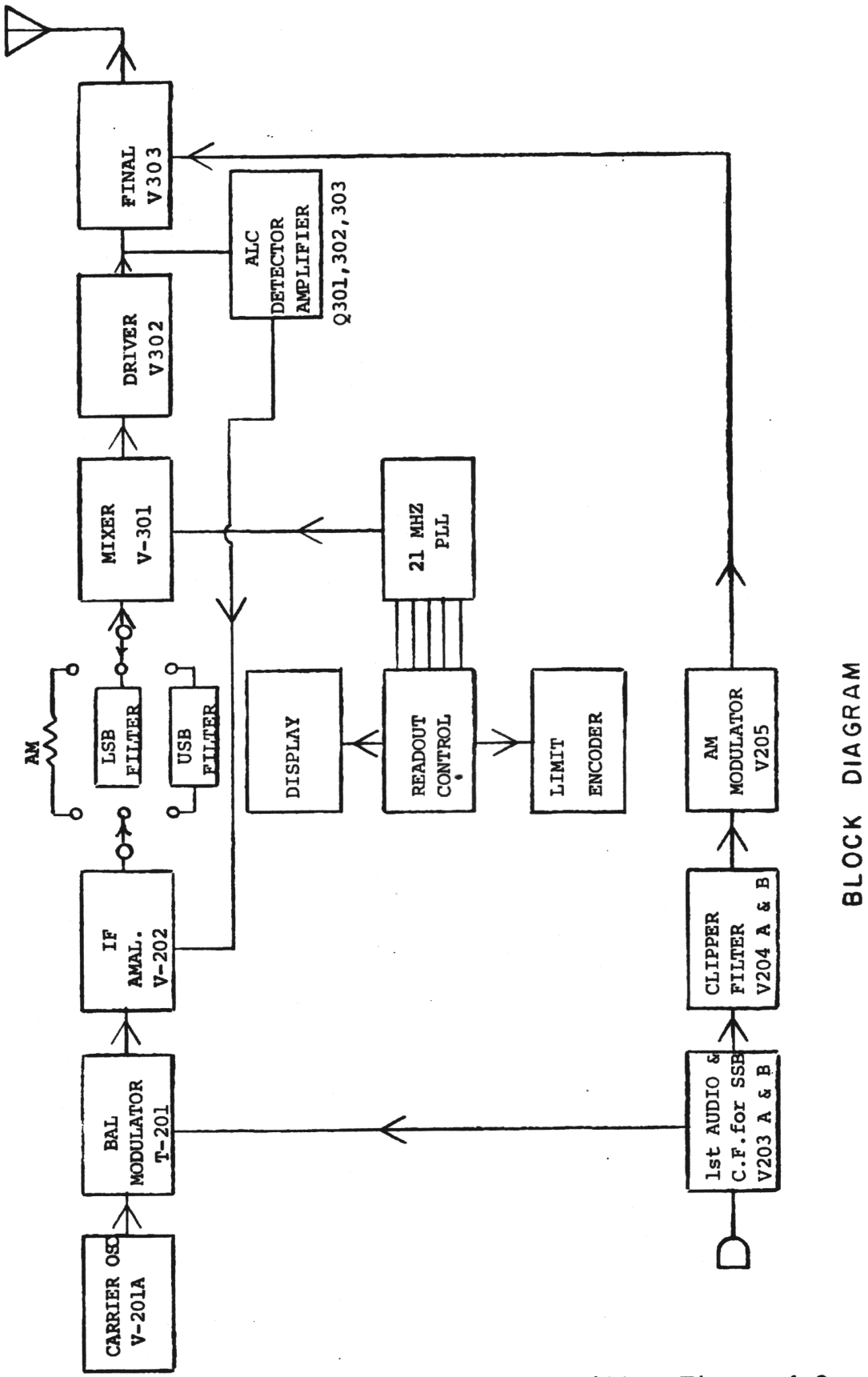
Audio detected by either the AM detector or the SSB product detector is applied through SW2-D to R6, the volume control. This signal is applied to V205B, the 1st Audio Amp and is raised to a level to drive V206, the Audio Output Amplifier. The output of V206 is transformer coupled to the speaker or via J1 to either an external speaker or low impedance headphones.

Also, at the junction of R6, Volume Control, and SW2-D is the network of C1 and R5 which comprise the Tone Control Circuit. By varying the Tone Control, the higher audio frequencies are attenuated.

4.2.11 POWER SUPPLY

The power supply located in the receiver supplies all voltages required for both the Transmitter and the Receiver. 117V AC is applied to the primary of T2 via the fuse (F1) and the Power Switch (part of Volume Control, R6). The secondary of T2 supplies four separate voltages; (1) the Green wires supply the 6.3V AC for all filaments in both the transmitter and receiver; (2) the Green-Yellow wires feed the full wave bridge rectifier D3. The +11V DC (@117V AC) is filtered by C5 and C6 and supply the receiver LED's and is also sent to the transmitter via J2 Pin 6; (3) the Red wires feed the full wave bridge rectifier D2. The high voltage from D2 is filtered by C3A. R9 drops the high voltage and through R8, supplies the receiver B+, +285V.

Also from R9, the transmitter high B+, is passed to the transmitter via J2 Pin 5 and the transmitter low B+ through RIO is passed to the transmitter via J2 Pin 3 (4) The Blue wires feed the full wave bridge rectifier Dl. The -45V DC output of Dl is filtered by C4 and feeds the transmitter final bias via J2 Pin 4 and a voltage regulator. The voltage regulator, Q301, supplies a regulated -9V to the ROM in the transmitter via J2 Pin 2.



Block Diagram GE IV Transmitter Figure 4.2

4.3 TRANSMITTER

4.3.1 GENERAL

The Browning Laboratories GE MK4 is a Phase Locked Loop 40-channel combination AM (Class C plate and screen-modulated) and SSB (Class AB1) Transmitter.

4.3.2 CARRIER OSCILLATOR AND MIXERS

Referring to the schematic and block diagram, the carrier oscillator frequency is generated at V201A for both AM and SSB at a frequency of 5.645 MHz. In the SSB Mode the cathode output of oscillator V201A is fed into the balanced modulator through a tuned circuit, and the double-sideband suppressed-carrier signal is amplified By V202. In the AM Mode the balanced modulator is bypassed through C207. The output of V202 is fed through a 5-MHz tuned circuit T202 to an 8-pole crystal lattice filter (FL201 or FL202). In AM the filters are bypassed by R609. The signal (sideband or AM carrier) is heterodyned to 27 MHz in mixer V301 with the 21-MHz PLL output from C113:
This the sum frequency of V201A (5 MHz) and PLL output (21 MHz).

The 27-MHz output of mixer V301 is coupled by two double-tuned circuits T301 and T302 to amplifier V302. The amplified signal is coupled to the output stage, V303, by another double-tuned circuit, T303.

The Pi Network output of V303 consists of C602, L602, and C603. L603 and C605 form an additional L.C. network to further attenuate any harmonics.

4.3.3 MODULATION

The audio for both AM and SSB modulation is fed through V203A and through C214, to the grid of V203B. In the SSB mode, V203B is a cathode follower with its output coupled through C216 to T201, the balanced modulator assembly.

In the AM mode, V203B becomes a triode amplifier; its output is fed into V204A and V204B, a clipper-limiter stage, to prevent over modulation. Audio output of V204B is connected to a Low Pass Filter (C218, L601 and C219) to remove the high frequency harmonics resulting from the clipping. The audio signal is then amplified by modulator V205 and transformer coupled to the plate and screen of V303, the output stage.

4.3.4 AUTOMATIC LEVEL CONTROL

In the SSB mode, an ALC (Automatic Level Control) circuit is used. This circuit consists of back-biased diodes D303 and D304. When the crest of the RF envelope exceeds the back bias on the diodes, a negative voltage is developed across R320. This voltage is buffered by Emitter follower Q301, amplified by Q302 and Q303, and filtered by R325 and C325. The resulting negative going voltage is applied as bias to V202, which reduces its gain.

4.3.5 PHASE LOCKED LOOP CIRCUIT DESCRIPTION

IC101 and associated components comprise a 6 MHz oscillator C-101 allows tuning of the 6 MHz crystal.

The 6 MHz output from Pin #2 of IC101 feeds the input (Pin#14) of IC102. IC102 is wired as a Divide-By-12, giving an output of 500 KHz at Pin #8. IC103 and IC104 are both wired as Divide-By-10's, giving an output of 5 KHz at Pin #12 of IC104.

At this point, we will leave the output of IC104 and will later see how it all ties together.

Q-105 and its associated components comprise a modified Colpits oscillator running at 21 MHz. The output is taken from the junction of the source of Q-105 and L-104, and fed to Q-103, which performs as an oscillator buffer. The 21 MHz output is via C-113 and is taken from the emitter of Q-103. Q-103 feeds Q-104, the Divide-By-N buffer.

PHASE LOCKED LOOP CIRCUIT DESCRIPTION (cont'd)

The 21 MHz signal from Q-104 is also fed to IC105 - 108, which are wired as high speed Divide-By-N counters. The Divide-By-N counters divide the 21 MHz signal in binary to provide a 5 KHz output at Pin #11 of IC108.

The 5 KHz pulses from IC108 and IC104 are fed to IC109, a digital phase detector. IC109 compares the two inputs and supplies an error voltage that depends on the frequency difference between the two inputs. Q-101 and its associated components amplify the error voltage and filter out the 5 KHz signals. The D.C. error voltage is passed through R-107 to D-111, a varactor. The varactor changes its value of capacitance depending on the amount of voltage impressed across it. Therefore, Q-105 and associated components, including D-111, make up a Voltage Controlled Oscillator, VCO.

The changing voltage on D-111 causes the frequency of the oscillator to change. The Divide-By-N circuit will divide the changing oscillator frequency by a constant number (which is programmed at its inputs by the ROM, IC410) until the output of IC108 Pin #11 is exactly the same as the output of IC104. When this happens, the error voltage will maintain at a constant amplitude. Thus, the voltage across D-111 will be constant and likewise, so will its value of capacitance, holding the oscillator at the desired frequency.

The Divide-By-N circuit divides in the range of 4264 to 4350 corresponding to the VCO output frequency range of 21.320 MHz to 21.760 MHz. The VCO output frequency is found for any output by:

(F out - 5.645) MHz, where the 5.645 MHz is the carrier frequency oscillator.

PHASE LOCKED LOOP CIRCUIT DESCRIPTION (cont'd)

The network of components to the bottom right of IC107, D-102, D-108, Q-106 and Q-107 comprise a gate which detects the absence of any "1's" in the binary code, and removes the voltage from the oscillator (thus killing the oscillator) so that an incorrect frequency cannot be generated

IC602 provides a regulated 5 volts to all the logic circuits. Q-102 operates both as an On-Off switch and a second regulator to supply the voltage to the oscillator and buffer stages.

IC504 is used as a lock detector. At IC109, Pins #2 and #4, is a sample of the pulses when the VCO must increase in frequency. Pins #11 and #13 give a sample of the pulses when the VCO must decrease in frequency. IC504, Section A, is a two input NAND gate, which compares to two sampled pulses from IC109 and will give an output which will be a pulsing Logic 1 when the PLL is out-of-lock and will be a Logic 0 when the PLL is in-lock. Following IC504, Section A, is an RC circuit which integrates the out-of-lock pulses and supplies the input of IC504, Section B, with a steady-state voltage (Logic 1 when out-of-lock and a Logic 0 when in-lock). IC504, Section B, performs as an inverter. Thus when in an out-of-lock condition. Section B's output will be at a Logic 0. Section B's output also supplies the necessary logic to blank the display when out-of-lock. IC504, Section C, also performs as an inverter, thus giving the same output as Section A, but controls the TR relay. Therefore, when out-of-lock, the TR relay cannot be operated, thus an out-of-band signal cannot be radiated.

4.3.6 READOUT AND DECODER CIRCUIT DESCRIPTION

IC406 and associated components comprise a pulse generator. IC406 generates pulses variable from approx. 148 milli-Sec. to 600 milli-Sec. via R-601, scan rate control. The pulses from Pin #3 of IC406 are fed into IC405 section C Pin #10. When a logic "1" is present on IC405 section C Pin #9, the output Pin #8 passes pulses to IC403 & 404 Pins #14. IC403 and IC404 are pre-settable BCD up-down counters. IC403 and IC404 are prewired to start on BCD code 01 when power is first applied.

When channel selector switch S-605 is moved to either the low or high position a ground condition is placed on the low or high input to IC409, a dual flip-flop, which transmits the input condition unchanged, to its respective output (pin #4 to pin #6 or pin #10 to pin #8). The output of IC409 controls IC405 sections A and B, which comprise a latch and will give the up-down counter its count direction control. Also when the channel selector switch is activated the output of IC409 will cause IC407 section A to act as an inverter enabling IC406 and IC405 IC405 section D. IC405 section D will thus enable IC404. The outputs of IC404 will count either up or down, depending on the state of IC405 sections A & B. IC403 and IC404 outputs are detected by IC401, 402, 410, 501 and 502. IC401 and 402 decode the BCD outputs of IC403 and 404 and encode the LED readouts I401 and I402 to display the channels from 01 to 40. IC410 performs as a code converter and converts the BCD info. from IC403 and 404 to the binary code required to encode the synthesizer.

IC501 and 502 also take the BCD information from IC403 and 404 and convert the BCD information into the decimal equivalent. IC503's inputs are strapped to detect channels 01 and 40. When channel 01 is detected, IC503 Pin #4 will go to a logic "0", lighting the low limit LED, 1403. The logic "0" from IC503 Pin #4 is integrated by the network of C403, R422, D404, and R420 and a negative pulse is placed on IC408 Pin #4.

This pulse sets the flip-flop section B output at Pin #5 to logic 1. IC407 section B will then change its output from logic "1" to logic "0" and thus disable IC405 section C. When IC405 section C is disabled, no pulses are allowed to pass and count down stops at channel 01. When the channel selector switch is placed in the UP position, IC405 section B output at Pin #6 will change from a logic "1" to a logic "0" and will reset IC408 section B flip-flop. At the same time the direction control of IC403 and 404 has been changed to a logic "0" via Pin #3 of IC405 section A, and IC403 and 404 will begin to count up from channel 01 to 40 or until the channel selector control has been released.

When channel 40 is detected by IC503, Pin #1 will change from a logic "1" to a logic "0" and thus light the high limit LED, 1404.This pulse is also integrated by the network of C405, R425, D405 and R424 and a logic "0" is placed on the set-line of flip-flop "A" of IC408 Pin #10.

The output of IC408, Pin #9, will change from a Logic 0 to a Logic 1, and IC407, Section B, Pin #13, will change from a Logic 1 to a Logic 0, again disabling IC405, Section C, from passing pulses. Thus the up-down counters IC403 and 404 will stop on Channel 40. When the channel selector switch is placed in the down position, pin #6, the output of IC405, Section B, will reset the A section flip-flop of IC408, thus allowing pulses to pass at IC405, Section C. This allows IC403 and 404 now to count down from Channel 40 to 01 or whenever the channel selector is released.

SECTION 5

ALIGNMENT

5.1 GENERAL

The Golden Eagle MK-IV Transmitter and Receiver are carefully aligned at the factory. Complete re-alignment is not recommended except technicians familiar with transistors and integrated circuits, possessing a 2nd Class FCC license and who have the necessary test equipment, and then only if absolutely necessary. Replacement of defective components in any stage should require re-alignment of that particular stage only.

5.2 RECEIVER ALIGNMENT

A. **455 KHz** Connect the test equipment as shown in Figure 5.1. Inject a modulated 455 KHz signal to the Junction of R113 and T201 (At Point A), through a 0.1 uF capacitor. Connect the VTVM to the junction of T-205, C217, R217, R219 and R229.Peak T201, 202, 203, 204 and 205 top and bottom cores for maximum on the DC-VTVM. Be sure that you have peaked to the outer peaks. (*One* slug of T201 may be tuned to inner peak if necessary for gain).

B. **VFO** Connect the test equipment as in A above. Inject 27.105 MHz (Channel 12) into the antenna terminal. Center the dial channel 12 to the line on the channel window opening. Set the Receiver for AM, CB-1 RF Gain Maximum CW, Squelch CCW, AGC pushed in, and ANL pushed in. Adjust L105 for a peak on the DC VTVM.

C. **OSCILLATOR.** Connect the oscilloscope to Pin 7 of V103B. Set the mode switch to CB2. Tune L-103 for highest level and adjust CCW down to 4V. P.P. Switch mode to CB-1 check for a slightly lower level.

RECEIVER ALIGNMENT (cont'd)

D. **27 MHz:** Connect as in item B above. Set the receiver for Channel 12 as in item B above. Adjust both top and bottom slug of T101 and T102 and L101 (one slug) for a peak reading on the DC VTVM.

1. Reset both receiver and signal generator for Channel 27 (27.275 MHz). Tune the bottom slug of T102 for a 1 volt increase on the DC VTVM. Note this voltage.
2. Reset both receiver and signal generator for Channel 1 (26.965 MHz). The voltage on the DC VTVM should be within 0.5v of the voltage noted in item 1 above. If not, adjust the top slug of T-102 until the voltage is approximately the same. Again, note this voltage.
3. Reset both receiver and signal generator again for Channel 12 (27.105 MHz). Recheck the DC VTVM for a voltage within 1 volt of the readings noted at Channels 1 and 27.

E. **DIAL CALIBRATION**

1. With the dial full CCW make sure the vertical line on the dial lines up with that on the window. If not reset the dial so that it does line up.
2. On 40-channel units (Channel 1 is on right side of the dial and the RF and oscillator sections are inside a shield cage which must be in place for dial calibration). Set the Receiver and signal generator to channel 12 and adjust L105 for peak S-meter reading.
3. Set Receiver and signal generator to Channel 23. Adjust C126 for peak on the S-Meter. Repeat Steps 2 and 3 until no further adjustment is required.
4. Set Receiver and signal generator to Channel 3.If necessary bend the right side near the Bakelite separator of outer sections of the movable portion of the main tuning capacitor (C8) until S-Meter peaks on Channel 3.
5. Repeat Steps 2, 3 and 4 until no further adjustment is necessary. For a 23-channel set use the same procedure but use Channel 3 in step 3 and Channel 22 in step 4.